

FIGURE 1 (PRIOR ART)

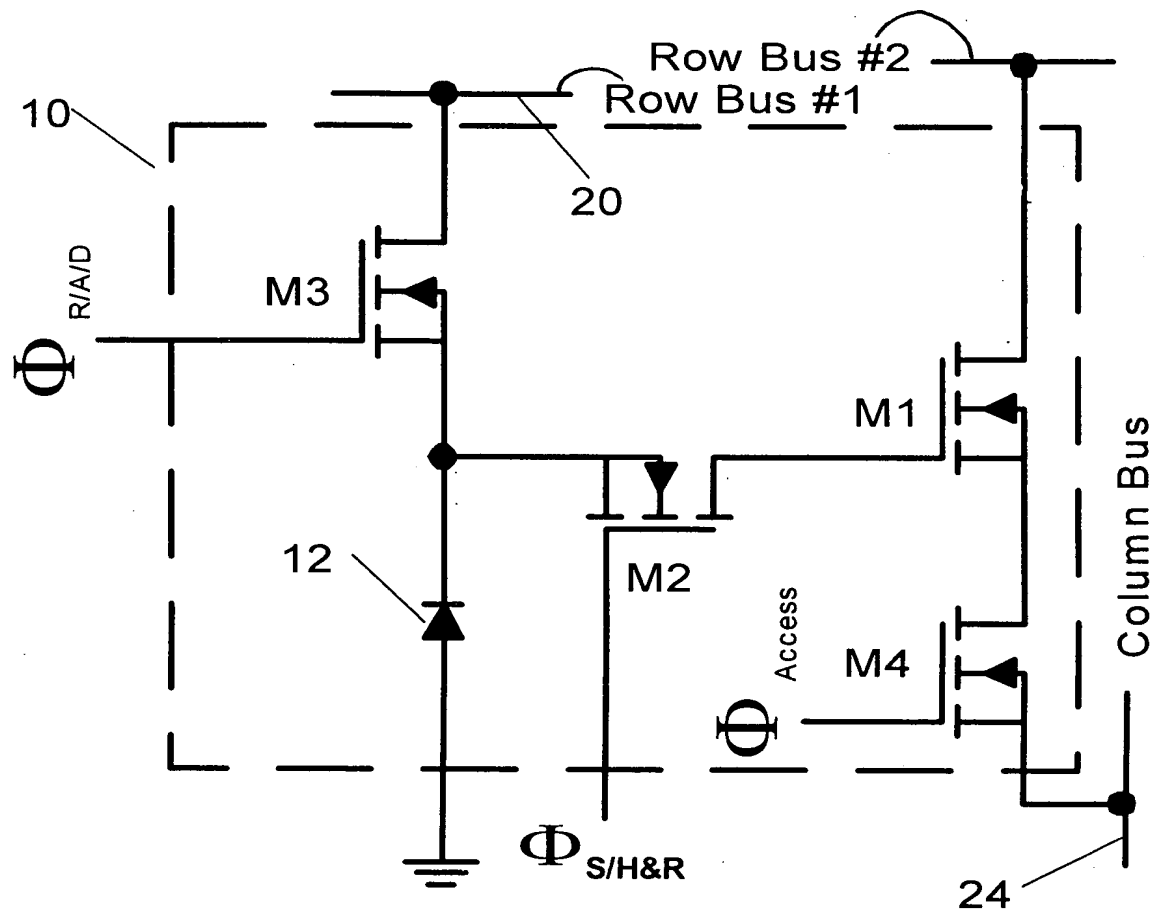


FIGURE 2

The diagram illustrates the internal structure and external circuitry of a 1T1R1C1 SRAM cell. The cell itself is shown in the top-left, consisting of a storage node (10) connected to a word line (20) through an access transistor (M2). The storage node is also connected to a bit line (22) through a read transistor (M1). A reset transistor (M3) is connected between the storage node and ground, controlled by a reset signal (Φ_{Reset}). A write transistor (M4) is connected between the storage node and ground, controlled by a write signal (Φ_{Access}). The storage node is also connected to a sense amplifier (24) through a sense transistor (M1).

The read/write circuitry is shown in the bottom-right. It includes a reset transistor (M201) controlled by Φ_{Reset} and a read transistor (M202) controlled by Φ_{Read} . The read transistor is connected to a sense amplifier (24) through a sense transistor (M101). The sense amplifier is connected to a sense line (22) through a sense transistor (M102). The sense line is also connected to a sense amplifier (24) through a sense transistor (M103). The sense amplifier is connected to a sense line (22) through a sense transistor (M104). The sense line is also connected to a sense amplifier (24) through a sense transistor (M105). The sense amplifier is connected to a sense line (22) through a sense transistor (M106).

FIGURE 3 (RESET)

The diagram illustrates the internal structure of a 1T1R1C1B1A1D1 memory cell (100). It is divided into several functional blocks:

- Access Transistor (M1):** Connected between the Row Bus (20) and the Word Line (22).
- Access Transistor (M4):** Connected between the Word Line (22) and the Bit Line (24).
- Reset Transistor (M201):** Connected between the Row Bus (20) and the Word Line (22). Its gate is controlled by Φ_{Reset} .
- Read Transistor (M202):** Connected between the Word Line (22) and the Bit Line (24). Its gate is controlled by Φ_{Read} .
- Amplifier (V_Amp):** A differential amplifier with inputs connected to the Word Line (22) and the Bit Line (24). Its output is connected to the Word Line (22).
- Reset Transistor (M101):** Connected between the Word Line (22) and the Bit Line (24). Its gate is controlled by Φ_{Reset} .
- Read Transistor (M103):** Connected between the Word Line (22) and the Bit Line (24). Its gate is controlled by Φ_{Read} .
- Drain Transistor (M105):** Connected between the Word Line (22) and the Bit Line (24). Its gate is controlled by Φ_{Drain} .
- Word Line (22):** A horizontal line connecting the various transistors.
- Bit Line (24):** A vertical line connecting the various transistors.
- Row Bus (20):** A horizontal line at the top of the cell.
- Control Signals:**
 - $\Phi_{R/A/D} = \text{OFF}$: Control signal for the Reset/Access/Drain transistors.
 - $\Phi_{Reset} = \text{OFF}$: Control signal for the Reset transistors.
 - $\Phi_{Read} = \text{OFF}$: Control signal for the Read transistors.
 - $\Phi_{Access} = \text{OFF}$: Control signal for the Access transistors.
 - $\Phi_{S/H\&R} = \text{OFF}$: Control signal for the Sense/Hold/Read transistors.
 - $\Phi_{Drain} = \text{OFF}$: Control signal for the Drain transistor.
- Biasing:**
 - V_{Inv_Bias} : Inverting bias voltage applied to the gates of M101 and M102.
 - V_{SF_Bias} : Sense/Feedback bias voltage applied to the gates of M103 and M104.
 - V_{Drain} : Drain bias voltage applied to the gate of M105.

FIGURE 4 (INTEGRATE)

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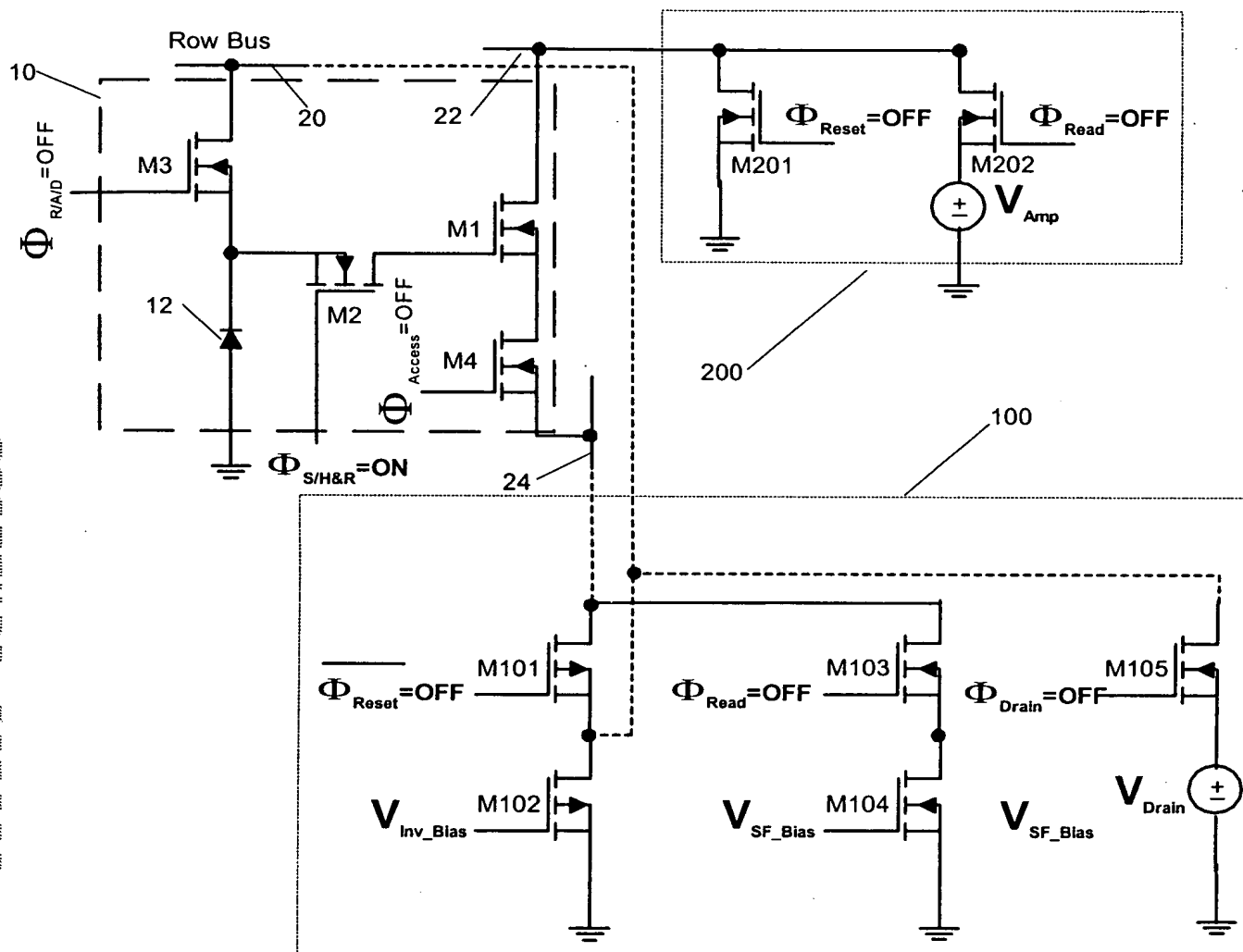


FIGURE 5 (SNAPSHOT)

[illegible]

FIGURE 6 (READ)

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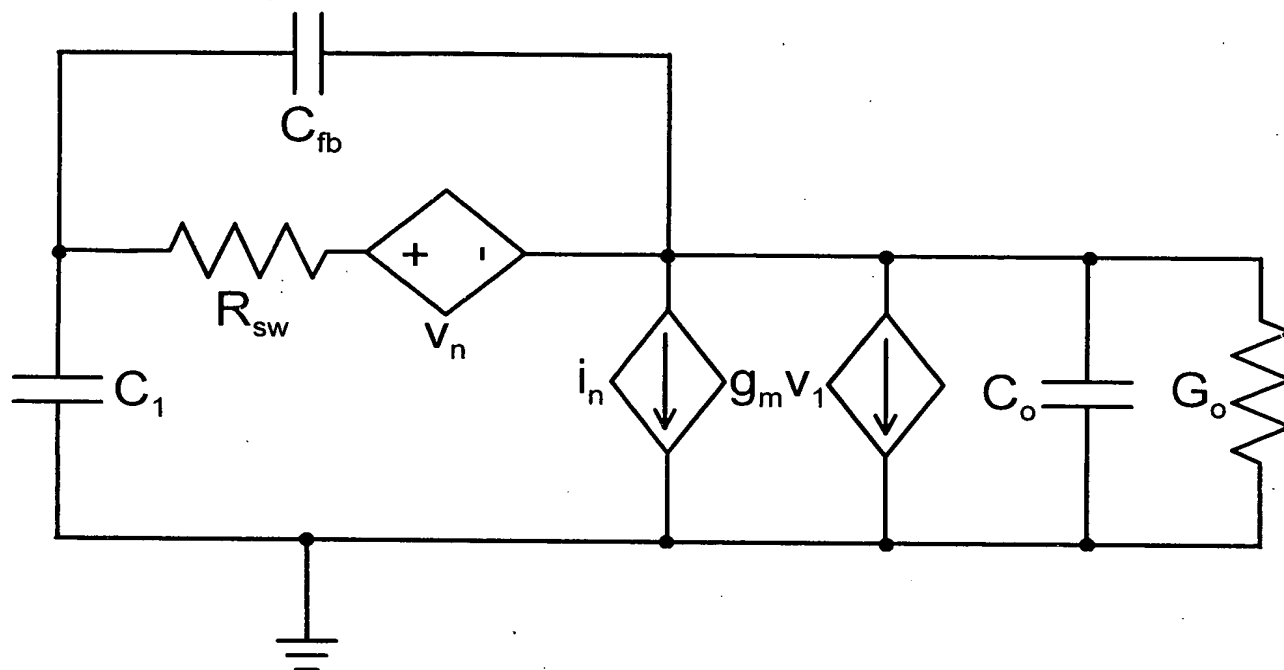


FIGURE 7

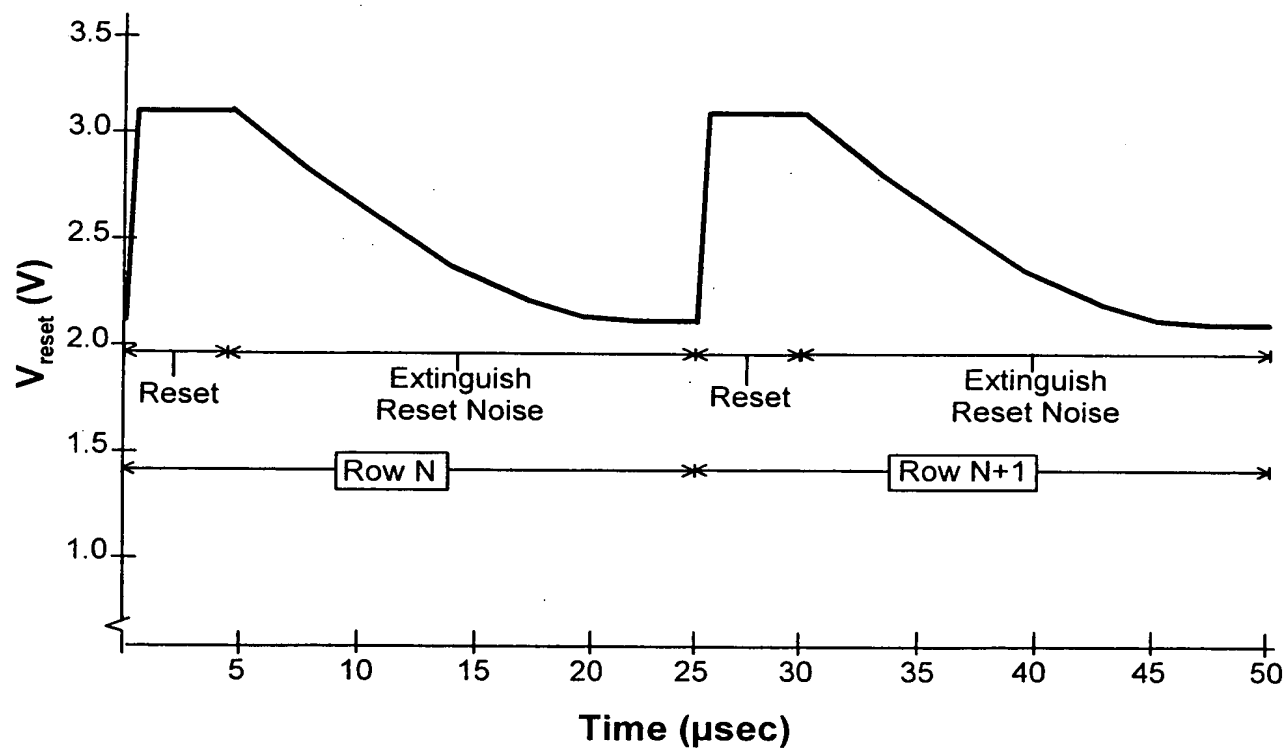


FIGURE 8